

Today's demand for higher speed systems is for increased performance, but with strong consideration for power usage. Traditionally, high-drive bus interface logic have been implemented in Bipolar technology, but recent years have witnessed strong demand for a CMOS counterpart series called FCT. In fact, FCT has evolved to deliver far greater performance (shorter propagation delays) than is available in Bipolar technology, thus becoming the only available avenue for very high-speed system designers. Maintaining the same high output drive capabilities as the Bipolar products (64mA sink), FCT circuits from Harris Semiconductor are now available with propagation delay down to 3.6ns (maximum) for some functions. However, speed improvements and power reduction has not come without some penalties in the form of a noise phenomena called "Ground Bounce."

Ground Bounce is the simultaneous switching noise of outputs during the logic HIGH to LOW transition and the resultant potential difference between the chip ground and the external ground plane. When several outputs switch simultaneously, the total build up of current in the common ground or V_{CC} lead inductance can be substantial. The noise becomes more pronounced as the output edge rate and the drive capability increase or as more current is switched through the ground lead.

Harris Semiconductor's FCT products are designed to have low ground bounce. The FCT family is TTL compatible and the output swing is limited to 3.4V TTL output swings instead of 5V. This reduces the discharge current through the ground lead and reduces maximum noise by 30% to 40%. Specially optimized control circuits are designed to gradually turn on the output driver to reduce ground bounce while achieving high speed. Optimized layout of the power and ground lines in the chip further reduces ground bounce.

Ground bounce and speed characterization were done on a special bench setup as shown in Figure 1. Ground bounce measurement was done with seven bits simultaneously driven from logic HIGH to logic LOW and the remaining bit tied to ground. The noise voltage waveform generated at the undriven bit (quiet bit) is measured and represents the worst case ground bounce noise. This is the standard setup and measurement in characterizing ground bounce. On system boards, the noise characteristics are usually much lower with proper board design.

A CD74FCT244T device in a plastic DIP package from Harris Semiconductor and two other suppliers were characterized with the setup as shown in Figure 1. Figures 2 and 3 compare the waveforms of the output voltage transitions and the corresponding ground bounce as observed at the undriven LOW output. Table 1 summarizes the results. The results show that Harris Semiconductor's FCT device has significantly lower ground bounce compared to the other suppliers. Other Harris FCT octal types with similar ground bounce performances include:

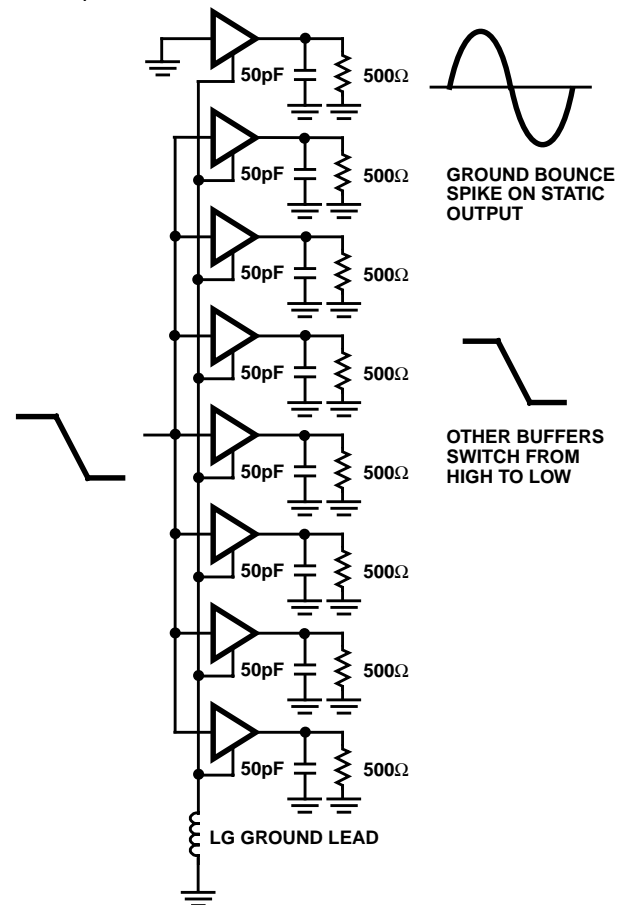


FIGURE 1. TYPICAL GROUND BOUNCE EVALUATION SETUP

CD74FCT240T	CD74FCT241T	CD74FCT245T
CD74FCT273T	CD74FCT373T	CD74FCT374T
CD74FCT377T	CD74FCT533T	CD74FCT534T
CD74FCT540T	CD74FCT541T	CD74FCT543T
CD74FCT544T	CD74FCT573T	CD74FCT574T
CD74FCT623T	CD74FCT640T	CD74FCT645T
CD74FCT646T	CD74FCT648T	CD74FCT651T
CD74FCT652T	CD74FCT825T	

Key to High Speed Low Noise Design

Ground bounce can only be minimized or circumvented, but rarely eliminated since the parasitic inductance cannot be totally removed from the package. Figure 4 shows a simplified circuit model to help explore several key factors which are critical for good ground bounce control design.

During the output HIGH to LOW transition, the sum of output load current and all switching current through the device flows through the ground lead and generates noise voltage. Several factors affect the amplitude of this voltage:

- Number of outputs switching simultaneously. The more outputs switching simultaneously, the more ground bounce.
- Magnitude of lead inductance. Higher lead inductance results in greater ground bounce. Thus, a package with less parasitic ground lead inductance would result in better noise performance.
- Output voltage swing. Higher output voltage swing would result in higher ground bounce. Thus, a CMOS compatible output with 5V V_{OH} would inherently result in higher noise than a TTL compatible output with lower V_{OH} voltage.

Output edge rate. The output edge rate determines how fast the current discharges through the ground lead inductor. Since the transient voltage across an inductor increases with the rate of change of the current, the faster the rate, the higher the noise. Thus it is very critical to control this output edge rate to get low noise performance.

Harris Semiconductor addresses these issues directly at the outset of the design. First, we design our FCT products to be TTL compatible. This limits the output swing to 3.4V instead of 5V. This reduces the maximum noise as the maximum output swing is lowered. To control the output edge rate without compromising speed, a proprietary control circuit is designed to gradually turn on the output driver to optimize the speed performance and ground bounce characteristics. Also, alternative package choices complement the high-speed low-noise design. Plastic DIP packages have the highest lead inductance and hence, the worst ground bounce characteristics. Packages like SOIC and QSOP have much lower lead inductance and hence, much lower ground bounce.

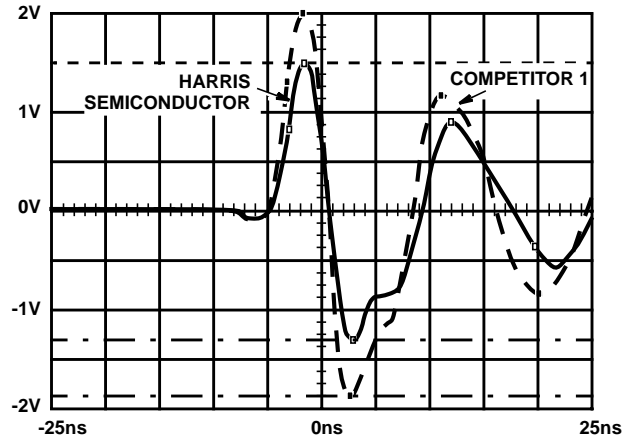


FIGURE 2. GROUND BOUNCE WAVEFORMS: HARRIS SEMICONDUCTOR vs COMPETITOR 1

TABLE 1. GROUND BOUNCE COMPARISON AT ROOM TEMPERATURE: HARRIS vs COMPETITORS 1 AND 2

UNIT	SPEED (ns)		GROUND BOUNCE (V)	
	t _{PHL}	t _{PLH}	POSITIVE	NEGATIVE
Harris, D Speed	2.84	2.88	1.52	1.28
Competitor 1, D Speed	2.92	3.08	2.04	1.88
Harris, C Speed	3.2	3.4	1.32	1.00
Competitor 2, C Speed	3.24	3.84	1.52	1.34

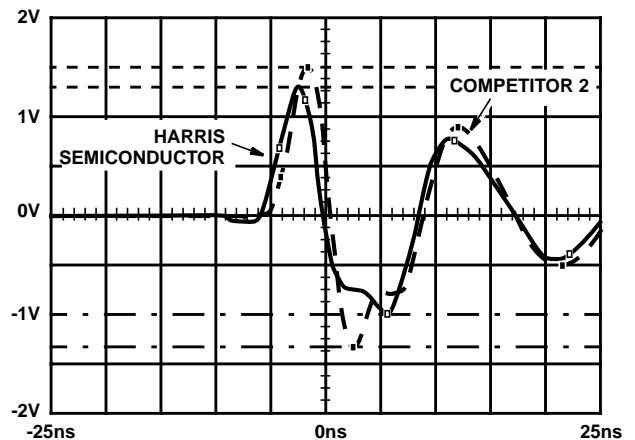


FIGURE 3. GROUND BOUNCE WAVEFORMS: HARRIS SEMICONDUCTOR vs COMPETITOR 2

Application Note 9646

Table 2 shows a comparison of package inductance and estimated ground bounce. It is evident that the surface mount packages (SOIC, QSOP) offer system designers the advantages of reduced board space, higher speed performance and lower ground bounce.

TABLE 2. GROUND BOUNCE PACKAGE COMPARISON

PACKAGE	GROUND LEAD INDUCTANCE	RELATIVE GROUND BOUNCE
PDIP	13.7nH	100%
SOIC	8.5nH	80%
QSOP	3.6nH	50%

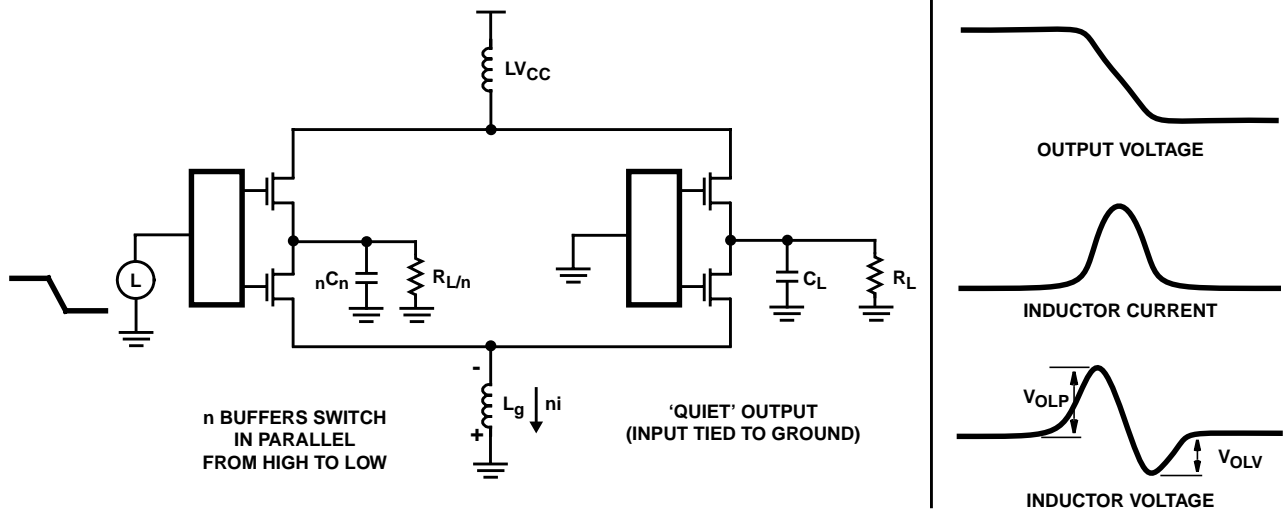


FIGURE 4. SIMPLIFIED CIRCUIT MODEL